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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/676,345, Patent No 6,922,082 B2	
	Filing Date	09/30/2003, Issued: 07/26/2005	
	First Named Inventor	Sapumal Wijeratne	
	Art Unit	2819	
	Examiner Name	Tan, Vibol	
Total Number of Pages in This Submission	5	Attorney Docket Number	110348-134107

ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> After Allowance Communication to TC
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT		
Firm Name	SCHWABE, WILLIAMSON & WYATT, P.C.	
Signature		
Printed name	William A. Holmes	
Date	11/06/2006	Reg. No. 59024

Certificate
NOV 14 2006
of Correction

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:

Wijeratne

Application No.: 10/676,345

Filed: September 30, 2003

Patent No.: 6,922,082 B2

Issued: July 26, 2005

For: SELECT LOGIC FOR LOW
VOLTAGE SWING CIRCUITS

Examiner: Vibol Tan

Art Group: 2819

Confirmation No. 7142

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Typed or Printed: Heather L. Adamson

Signature:  Date: 11/06/2006

Attn: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION

Dear Sir:

Upon review of the above-referenced Letters Patent, Applicant noted errors that are mistakes of the Applicant. The errors are as follows:

In the Drawings:

Fig. 1, "LVS MUX 10" should read --LVS CIRCUIT 10--;

Fig. 2, "LVS MUX 20" should read --LVS CIRCUIT 20--;

Fig. 2, "BUFFERS" should read --BUFFERING INVERTERS--;

Fig. 3, "n1" should read --N1--;

Fig. 3, "n2" should read --N2--;

Fig. 3, "n3" should read --N3--;

Fig. 3, "p1" should read --P1--;

Fig. 3, "p2" should read --P2--;

Fig. 3, "INPUT/OUTPUT DEVICE 142" should read -- INPUT/OUTPUT MODULE
142--;

In the Claims:

Col. 3, line 35, "...signals LCS-IN1, LCS-IN2, and LCS-IN3 respectively..." should
read --...signals LVS-IN1, LVS-IN2, and LVS-IN3 respectively....--;

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Col. 6, line 51, "...signal 90 provides..." should read --...signal 94 provides...--;
Col. 8, line 4, "...the inverters 46, are..." should read --... the buffering inverters
52, are...--;
Col. 9, line 52, "...the LVS circuit 12." should read --...the LVS circuit 10. --;
Col. 9, line 67, "...art select logic circuit 10..." should read --...art LVS circuit
10...--;
Col. 10, line 34, "...memory 146 include..." should read --...memory 136 include
...--; and
Col. 13, line 7, "...a central processor unit..." should read --...a central
processing unit...--;


Enclosed is a Certificate of Correction (in duplicate) and it is respectfully
requested that a Certificate of Correction be issued. This request for correction is made
under the provisions of 37 C.F.R. § 1.323.

Also enclosed is a check in the amount of \$100.00 for payment of the fee as set
forth in 37 C.F.R. § 1.20(a).

The Commissioner is hereby authorized to charge shortages or credit
overpayments to Deposit Account No. 500393.

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: 11/06/2006



William A. Holmes
Registration No. 59,024

Pacwest Center, Suite 1900
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Telephone: 503-222-9981

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 1 of 1

PATENT NO. : 6,922,082 B2

APPLICATION NO.: 10/676,345

ISSUE DATE : 07/26/2005

INVENTOR(S) : Wijeratne

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Drawings:

Fig. 1, "LVS MUX 10" should read --LVS CIRCUIT 10--;

Fig. 2, "LVS MUX 20" should read --LVS CIRCUIT 20--;

Fig. 2, "BUFFERS" should read --BUFFERING INVERTERS--;

Fig. 3, "n1" should read --N1--;

Fig. 3, "n2" should read --N2--;

Fig. 3, "n3" should read --N3--;

Fig. 3, "p1" should read --P1--;

Fig. 3, "p2" should read --P2--;

Fig. 3, "INPUT/OUTPUT DEVICE 142" should read -- INPUT/OUTPUT MODULE 142--;

In the Claims:

Col. 3, line 35, "...signals LCS-IN1, LCS-IN2, and LCS-IN3 respectively..." should read --...signals LVS-IN1, LVS-IN2, and LVS-IN3 respectively...--;

Col. 6, line 51, "...signal 90 provides..." should read --...signal 94 provides...--;

Col. 8, line 4, "...the inverters 46, are..." should read --... the buffering inverters 52, are...--;

Col. 9, line 52, "...the LVS circuit 12." should read --...the LVS circuit 10. --;

Col. 9, line 67, "...art select logic circuit 10..." should read --...art LVS circuit 10...--;

Col. 10, line 34, "...memory 146 include..." should read --...memory 136 include ...--; and

Col. 13, line 7, "...a central processor unit..." should read --...a central processing unit...--.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW Fifth Ave., Suite 1900
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- Fig. 3, "n2" should read --N2--;
- Fig. 3, "n3" should read --N3--;
- Fig. 3, "p1" should read --P1--;
- Fig. 3, "p2" should read --P2--;
- Fig. 3, "INPUT/OUTPUT DEVICE 142" should read -- INPUT/OUTPUT MODULE 142--;

In the Claims:

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- Col. 10, line 34, "...memory 146 include..." should read --...memory 136 include ...--; and
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